Complete 10-Bit, 25MHz CCD Signal Processor

● FEATURES

25 MSPS correlated double sampler (CDS)
6dB to 42dB 10-bit variable gain amplifier (VGA)
Low noise optical black clamp circuit
Preblanking function
10-bit 25 MSPS A/D converter
No missing code guaranteed
3-wire serial digital interface
3V single-supply operation
Space-saving 5mm x 5mm QFN-32 package

● APPLICATIONS

CCTV cameras
Portable CCD imaging devices
Digital still cameras
Digital video camcorders
PC cameras

●GENERAL DESCRIPTION

The IT9943 are complete analog signal processors for CCD applications. It feature a 25MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The signal chain for the IT9943 consists of a correlated double sampler (CDS), a digitally controlled variable gain amplifier (VGA), and a black level clamp. The IT9943 offers 10-bit ADC resolution.

The internal registers are programmed through 3-wire serial digital interface. Programmable features include gain adjustment, black level adjustment, input clock polarity, and power-down modes. The IT9943 operate from a single 3V power supply, typically dissipate 79mW, and are package in space-saving 32-lead QFN packages.

FUNCTION BLOCK DIAGRAM

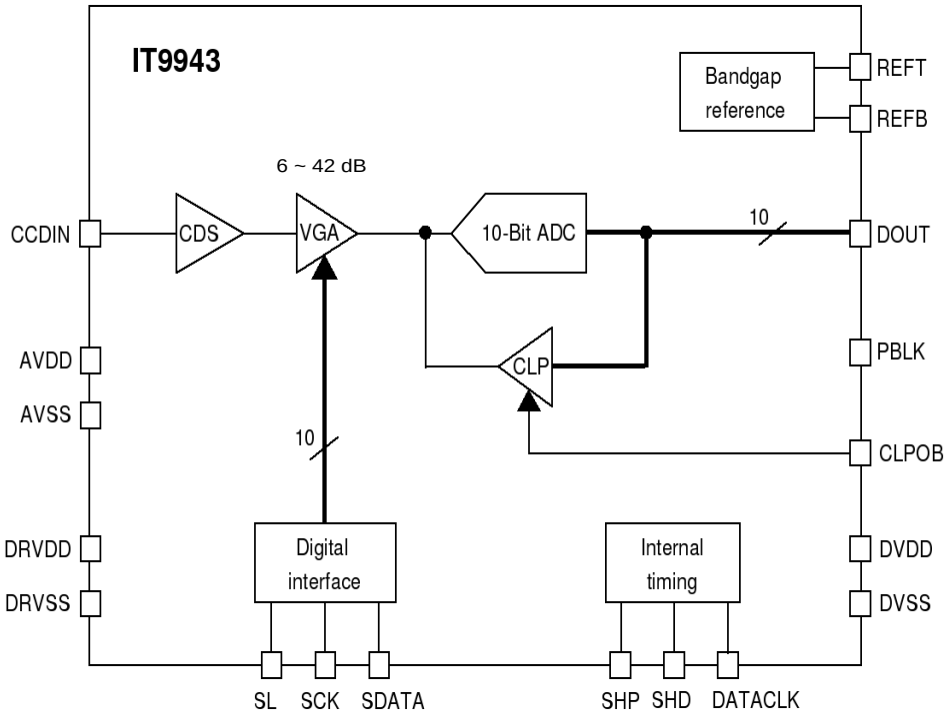

Fig 1. Functional block diagram

SPECIFICATIONS

● GENERAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3V, f_{SAMP} = 25MHz, unless otherwise noted.

Table 1.

Parameter	Min.	Typ.	Max.	Unit
TEMPERATURE RANGE				
Operating	-20		85	^{o}C
Storage	-65		150	^{o}C
POWER SUPPLY VOLTAGE				
Analog,Digital,Digital Driver	2.8		3.6	V
POWER CONSUMPTION				
Normal Operation		79		mW
Power-Down Mode		147		uW
MAXIMUM CLOCK RATE			25	MHz

● DIGITAL SPECIFICATIONS

DRVDD = DVDD = 2.7V, C_L = 20pF, unless otherwise noted.

Table 2.

Parameter	Symbol	Min.	Typ.	Max.	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		uA
Low Level Input Current	I_{IL}		10		uA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage, IOH=2mA	V_{OH}	2.2			V
Low Level Output Voltage, IOL=2mA	V_{OL}			0.5	V

● SYSTEM SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = DVDD = DRVDD = 3V, f_{SAMPLE} = 25MHz, unless otherwise noted.

Table 3.

Parameter	Min.	Typ.	Max.	Unit
CDS				
Maximum Input Range before Saturation[1]		1		Vpp
Allowable CCD Reset Transient		500		mV
Maximum CCD Black Pixel Amplitude		100		mV
VARIABLE GAIN AMPLIFIER (VGA)				
Gain Control Resolution		1024		Steps
Gain Monotonicity		Guaranteed		
Gain Range (See Fig.6 VGA gain curve)				
Minimum Gain		5.8		dB
Maximum Gain	40	42.4		dB
Gain Accuracy		+- 1		dB
BLACK LEVEL CLAMP				
Clamp Level Resolution		256		Steps
Clamp Level				
Minimum Clamp Level		0		LSB
Maximum Clamp Level		63.5		LSB
A/D CONVERTER				
Resolution	10			Bits
Differential Nonlinearity (DNL)		0.5		LSB
No Missing Codes		Guaranteed		
Data Output Coding		Straight binary		
Full-Scale Input Voltage		2		V
VOLTAGE REFERENCE				
Reference Top Voltage (REFT)		2.1		V
Reference Bottom Voltage (REFB)		1.1		V

NOTES :

[1] Input signal characteristics defined as follows: