8-Bit 2.5MHz R2R D/A Converter

General Description:

The IT88347A is realized by CMOS processes. It contains 8 R-2R D/A converter modules with 8-bit resolution. The output voltage range of each channel can achieve full voltage swing (from 2.7V to 3.6V or 4.5V to 5.5V) when VCC equal to VDD and VSS equal to GND. The digital data is serially input into individual channel by three control pin (DI, CLK and DO). The 8 operational amplifiers are built in each channel of D/A converter, which is helpful to drive

Features:

. 8 channel R-2R type D/A converter with 8-bit resolution.

. The inputs data in 12-bit serial mode, it just needs three control signals DI, LD, and CLK.

. Max. clock frequency … 2.5MHz.

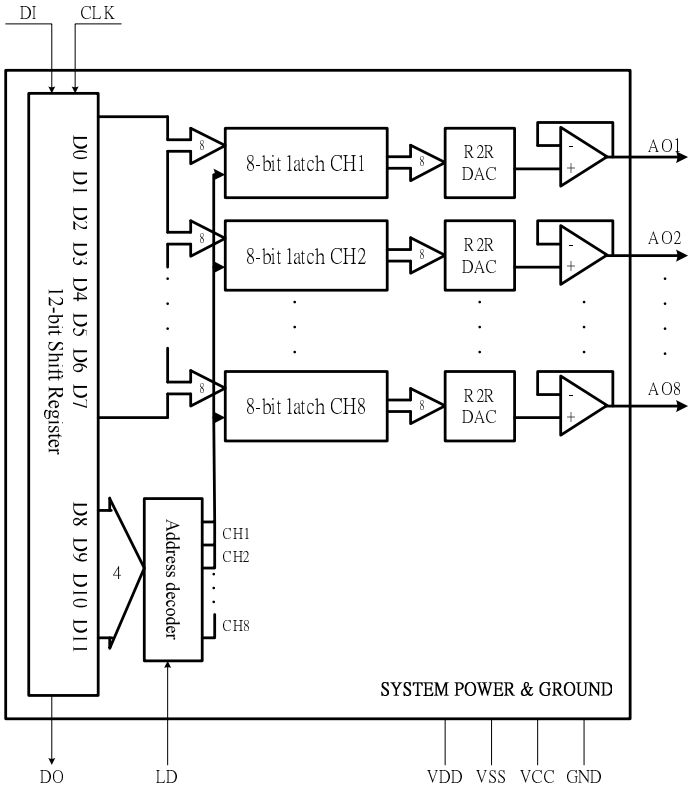
. Power consumption (Analog power supply)

… < 2 mA@VDD=VCC=3.6V, no load.

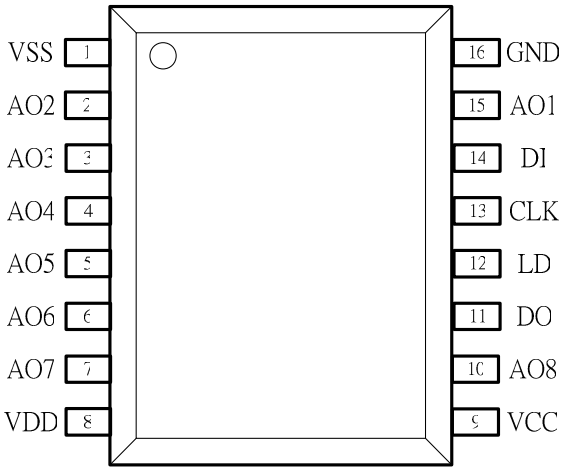
. Max. sink /source current ... 1.0mA

. Analog output range … Full voltage swing if VDD=VCC and VSS=GND.

Functional Block Diagram:



Pin Assignment: TSSOP-16

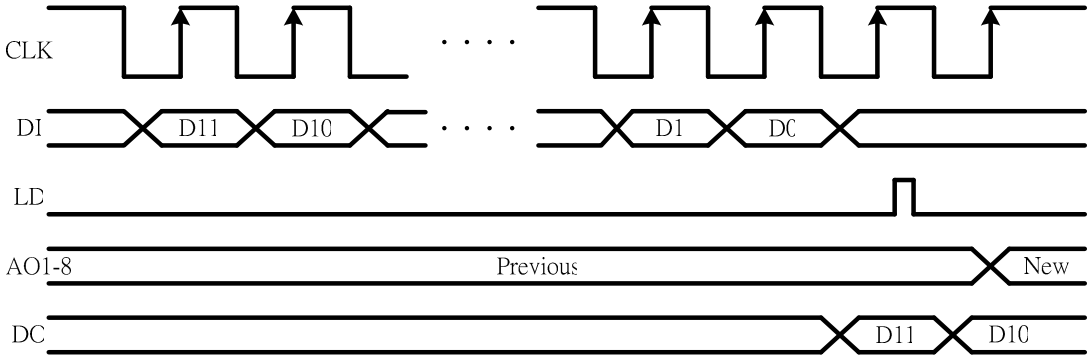


IT88347A

Pin Information:

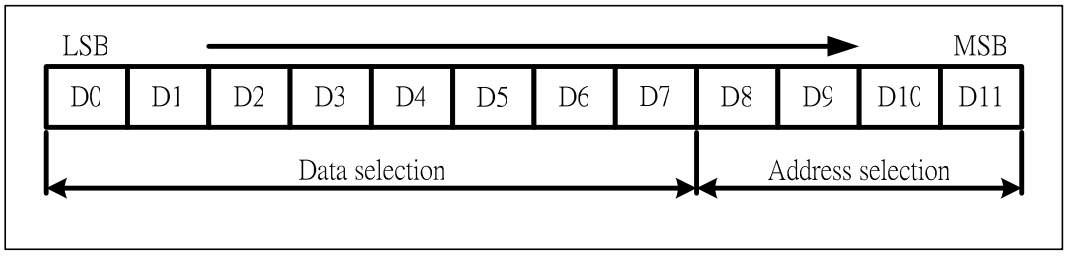
PIN NO.	PIN NAME	PIN TYPE	DESCRIPTION
1	VSS	POWER	Analog ground pin
8	VDD	POWER	Analog power supply pin
9	VCC	POWER	Digital power supply pin
16	GND	POWER	Digital ground pin
11	DO	OUTPUT	Serial Digital Data output pin.
12	LD	INPUT	Data Load pin. The data of Shift Register is loaded into the Address decoder and Data latch when it goes high
13	CLK	INPUT	Clock input pin
14	DI	INPUT	Serial Digital Data input pin
15	AO1	ANALOG OUTPUT	8-bit DAC outputs
2	AO2		
3	AO3		
4	AO4		
5	AO5		
6	AO6		
7	AO7		
10	AO8		

Data Setting Format:



Data Configuration:

The data and address is set by 12-bit serial input signal contains a 8-bit data output and a 4-bit address selection.



Data Conversion:

D0	D1	D2	D3	D4	D5	D6	D7	DAC Output
0	0	0	0	0	0	0	0	VSS
1	0	0	0	0	0	0	0	VSS+V_{LSB}×1
0	1	0	0	0	0	0	0	VSS+V_{LSB}×2
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	VDD

Note: V_{LSB} = (VDD- VSS)/255

Address Conversion:

D8	D9	D10	D11	Address selection
0	0	0	0	NA
0	0	0	1	AO1 Selection
0	0	1	0	AO2 Selection
0	0	1	1	AO3 Selection
0	1	0	0	AO4 Selection
0	1	0	1	AO5 Selection
0	1	1	0	AO6 Selection
0	1	1	1	AO7 Selection
1	0	0	0	AO8 Selection
1	0	0	1	NA
1	0	1	0	NA
1	0	1	1	NA
1	1	0	0	NA
1	1	0	1	NA
1	1	1	0	NA
1	1	1	1	NA

Electrical Characteristics:

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Unit	Min	Typ	Max
Digital Power Supply	VCC	VCC ≥ VDD VDD – VSS ≥ 2.5 VSS ≥ GND	V	2.7		5.5
	GND				0	
Analog Power Supply	VDD		V	2.7		VCC
	VSS			GND		VCC–2.7
Max. Output Source / Sink Current	I_{AO}	VCC=VDD=3V VSS=GND=0V	mA	–1.0		1.0
Oscillation Limit Output Capacity	C_{OL}		uF		1.0	
Operating Temperature	Ta		°C	–20		+85

DC Characteristics:

(1) Digital block						
Parameter	**Symbol**	**Condition**	**Unit**	**Min..**	**Typ.**	**Max.**
Digital Current	I_{CC}	CLK=1MHz without load	mA			0.01
Digital Input Low Voltage	V_{IL}		V			0.2VCC
Digital Input High Voltage	V_{IH}		V	0.8VCC		
(2) Analog block						
Parameter	**Symbol**	**Condition**	**Unit**	**Min..**	**Typ.**	**Max.**
Analog Current	I_{DD}	No load	mA			0.8
Analog Output Drive Range (VCC=VDD=3.3V / VSS=GND)	V_{AOH}	I_{AOH}=0uA	V	VDD - 0.1	VDD	VDD + 0.1
		I_{AOH}=-1mA	V	VDD - 0.3	VDD	VDD + 0.3
Analog Output Sink Range (VCC=VDD=3.3V / VSS=GND)	V_{AOL}	I_{AOH}=0uA	V	VDD - 0.1	VDD	VDD + 0.1
		I_{AOH}=+1mA	V	VDD - 0.3	VDD	VDD + 0.3
Resolution	Res	VCC=3.3V / VDD=3.3V VSS=0V/ No Load	Bit		8	
Integral Non-Linearity (Note 1)	INL		LSB	-1		+1
Differential Non-Linearity (Note 1)	DNL		LSB	-0.5		+0.5

Note 1: DNL and INL performance is better when the power supply is 4.5V to 5.5V.

Timing Specification:

Parameter	Symbol	Condition	Unit	Min.	Typ.	Max.
Clock Rate	T_{CLK}		ns	400	1000	
Load Strobe Pulse Width	T_{LDP}		ns		200	
Analog Output Settling Time	T_{AOS}	Analog output load RAL=10k / CAL=50pF	us			200
Digital Output Delay Time	T_{DOD}	CL=100pF	ns			170

Timing Diagram: